FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

OIPE JC13 NOV 17 2003 PATENT & TRADEMARK OFFICE

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
10971278-3	10/627,279	

APPLICANT: Richard B. Zeng

FILING DATE: July 25, 2003

GROUP: 2124

REFERENCE DESIGNATION — U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
CD	1A	5,734,599	03/31/1998	Lee et al.	
CD	1B	09/510,271		Zeng	
CD	1C	09/510,274		Zeng	
CD	1D	4,495,593	01/1985	Ware	
CD	1E	4,769,219	01/1989	Williams	
CD	1F	5,854,757	12/1998	Dierke	
CD	1G	5,121,352	06/1992	Hesson	
CD	1H	6,366,944	04/2002	Hossain et al.	
CD	1I	5,303,176	04/1994	Hrusecky et al.	
CD	1J	4,989,168	01/1991	Kuroda et al.	
CD	1K	5,734,599	03/1998	Lee et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
CD	1L	EP0318957 A2	06-07-1989	Fujitsu Limited		
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

CD	1Q	United Kingdom Search Report for application No. GB 0104187.0, December 3, 2001
CD	1R	LARSSON-EDEFORS P. et al., "Most-Significant-Bit-First Serial/Parallel Multipliers", August 1998, IEEE Proc-Circuits Devices Systems, Vol. 145 No. 4, page 278-284.
CD	1S	SATYANARAYANA, J. et al., "Systematic Analysis of Bounds on Power Consumption in Pipelined and Non-pipelined Multipliers", 1996, IEEE, page 492-499.

EXAMINER: [signature]

DATE CONSIDERED: 8/30/04

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NOV 17 2004
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REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
CD	2A	6,029,187	02/2000	Vergauwhede	
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
	2H				
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

CD	2Q	NAYAK, S.S. et al., "High Throughput VLSI Implementation of Discrete Orthogonal Transforms Using Bit-Level Vector-Matrix Multiplier", May 1999, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 46 No. 5, page 655-658.
CD	2R	SUNDER, S. et al., "Two's Complement Fast Serial-Parallel Multiplier", February 1995, IEEE Proc. Circuits Devices Systems Vol. 142 No. 1, page 41-44.
	2S	

EXAMINER [signature] DATE CONSIDERED 8/30/04

Rev 10/03 (PTO1449)

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NOV 17 2003
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UC13

PATENT APPLICATION

ATTORNEY DOCKET NO. 10971278-3

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Richard B. Zeng	**Confirmation No.:**	
Application No.:	10/627,279	**Examiner:**	
Filing Date:	July 25, 2003	**Group Art Unit:**	

Title: LINEAR SUMMATION MULTIPLIER ARRAY IMPLEMENTATION FOR BOTH SIGNED AND UNSIGNED MULTIPLICATION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97 (c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: Nov. 12, 2003

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number _____ on _____
Number of pages:

Typed Name: John Pallivathukal

Signature: _____

Rev 10/03 (IDSCERT)

Respectfully submitted,

Richard B. Zeng

By _____
Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. **44,034**

Date: **Nov. 12, 2003**

Telephone No.: **(214) 855-8007**